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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/666,317	09/19/2003	David Mui	8377/ETCH/SILICON/JB	7907
55649	7590	11/02/2005	EXAMINER	
MOSER IP LAW GROUP / APPLIED MATERIALS, INC. 1040 BROAD STREET 2ND FLOOR SHREWSBURY, NJ 07702			CHEN, ERIC BRICE	
			ART UNIT	PAPER NUMBER
			1765	

DATE MAILED: 11/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary

Application No.

10/666,317

Applicant(s)

MUI ET AL.

Examiner

Eric B. Chen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 6 September 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-23 and 29-33 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-23 and 29-33 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claim 1-13, 15, 17-23, 29-30, and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tao et al. (U.S. Patent No. 6,620,631) in view of Wolf et al., *Silicon Processing for the VLSI Era*, Vol. 1, Lattice Press (1986) ("Wolf I").

3. As to claim 1, Tao discloses a method for controlling dimensions of structures formed on a substrate using an etch process, comprising: providing the substrate (10) (column 6, lines 37-41) having a patterned etch mask (14a/14b/14c/14d/14e) (column 7, lines 35-37) formed thereon (Figure 1); measuring dimensions of elements of the mask (14a/14b/14c/14d/14e) on the substrate (10) (column 8, lines 50-61); adjusting a process recipe for an etch process using the results of measuring the dimensions (column 9, lines 11-15); and forming structures on the substrate by performing the etch process that uses the adjusted process recipe (column 10, lines 42-51; Figure 2).

4. Tao does not expressly disclose that the etch is for an overetch step of the etch process. However, Wolf I teaches that due to etch non-uniformities, an overetch (or additional etching) may be required for the complete removal of etched film (page 523). Therefore, it would have been obvious to one of ordinary skill in the art at the time the

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invention was made to use an overetch step of the etch process. One who is skilled in the art would be motivated to completely removal a film to be etched, for a more precise pattern transfer (page 521).

5. As to claim 2, Tao discloses that the substrate (10) is a semiconductor wafer (column 6, lines 37-41).

6. As to claim 3, Tao discloses that the mask (14) is a patterned hard etch mask or a patterned photoresist mask (column 7, lines 35-47).

7. As to claim 4, Tao discloses that the structures are formed in at least one material layer (12) disposed beneath the mask (column 6, lines 33-36; Figures 1-2):

8. As to claim 5, Tao discloses that the dimensions are smallest widths of the elements (column 5, lines 15-20).

9. As to claim 6, Tao discloses that the dimensions are measured using a non-destructive measuring technique (column 8, lines 50-61).

10. As to claim 7, Tao discloses that the measuring technique is an optical measuring technique (column 8, lines 50-61).

11. As to claim 8, Tao discloses that the measuring step and the forming step are performed using processing modules of a single substrate processing system (column 5, lines 38-44).

12. As to claim 9, Tao discloses that the adjusting step comprises calculating an adjustment for the process recipe of the etch process (column 9, lines 11-15).

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13. As to claim 10, Tao discloses that the adjustment is an adjustment for at least one parameter related to a thickness of a film of the material removed from sidewalls of the structures during the etch process (column 9, lines 20-32).

14. As to claim 11, Tao discloses that the at least one parameter is selected from a group consisting of a duration of time for overetching the structures, a flow rate and/or pressure of an etchant gas or gases, a plasma source power, a substrate bias power, a material of the structures and a thickness of sidewalls of the structures (column 9, lines 20-37).

15. As to claim 12, Tao discloses a method for controlling dimensions a gate structure of a field effect transistor (column 5, lines 56-63) formed on a substrate using an etch process, comprising: providing the substrate (10) (column 6, lines 37-41) having a patterned etch mask (14a/14b/14c/14d/14e) (column 7, lines 35-37) formed upon a film stack of the gate structure (12) (column 7, lines 21-31; Figure 1); measuring dimensions of elements of the mask (14a/14b/14c/14d/14e) on the substrate (10) (column 8, lines 50-61); adjusting a process recipe for an etch process of etching a layer of the film stack using the results of measuring the dimensions (column 9, lines 11-15); and forming the structures in the layer by performing the etch process that uses the adjusted process recipe (column 10, lines 42-51; Figure 2).

16. Tao does not expressly disclose that the etch is for an overetch step of the etch process. However, Wolf I teaches that due to etch non-uniformities, an overetch (or additional etching) may be required for the complete removal of etched film (page 523). Therefore, it would have been obvious to one of ordinary skill in the art at the time the

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invention was made to use an overetch step of the etch process. One who is skilled in the art would be motivated to completely removal a film to be etched, for a more precise pattern transfer (page 521).

17. As to claim 13, Tao discloses that the layer (12) is selected from a group consisting of a gate conductor layer and a gate electrode layer (column 7, lines 21-31).

18. As to claim 15, Tao discloses that the mask (14) is a patterned hard etch mask or a patterned photoresist mask (column 7, lines 35-47).

19. As to claim 17, Tao discloses that the dimensions are smallest widths of the elements (column 5, lines 15-20).

20. As to claim 18, Tao discloses that the dimensions are measured using a non-destructive measuring technique (column 8, lines 50-61).

21. As to claim 19, Tao discloses that the measuring technique is an optical measuring technique (column 8, lines 50-61).

22. As to claim 20, Tao discloses that the measuring step and the forming step are performed using processing modules of a single substrate processing system (column 5, lines 38-44).

23. As to claim 21, Tao discloses that the adjusting step comprises calculating an adjustment for the process recipe of the etch process for etching the layer (column 9, lines 11-15).

24. As to claim 22, Tao discloses that the adjustment is an adjustment for at least one parameter related to a thickness of a film of the material removed from sidewalls of the layer during the etch process (column 9, lines 20-32).

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25. As to claim 23, Tao discloses that the at least one parameter is selected from a group consisting of a duration of time for overetching the structures, a flow rate and/or pressure of an etchant gas or gases, a plasma source power, a substrate bias power, a material of the structures and a thickness of sidewalls of the structures (column 9, lines 20-37).

26. As to claim 29, Tao discloses measuring the dimensions of elements of the mask on the substrate in a number of regions (14a/14b/14c/14d/14e) (column 6, lines 33-36; Figure 1).

27. As to claims 30, Tao discloses measuring the dimensions of elements of the mask on the substrate at least in about five regions (14a/14b/14c/14d/14e) (column 6, lines 33-36; Figure 1).

28. As to claims 32, Tao discloses measuring the dimensions of elements of the mask on the substrate at least in about five regions. (14a/14b/14c/14d/14e) (column 6, lines 33-36; Figure 1).

Claim Rejections - 35 USC § 103

29. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tao in view of Wolf I, in view further view of Wolf, *Silicon Processing for the VLSI Era*, Vol. 4, Lattice Press (2002) ("Wolf IV"), in further view of Streetman, *Solid State Electronic Devices*, Prentice Hall (1990).

30. As to claim 14, Tao discloses that the gate electrode layer comprises doped polysilicon (column 7, lines 23-25).

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31. Tao does not expressly disclose that the gate conductor layer comprises WSi. However, Wolf I teaches for field effect transistor devices, delays in interconnect switching can be reduced by incorporating low resistivity materials (page 384). Moreover, refractory silicides, such as WSi₂, TiSi₂, MoSi₂, TaSi₂, are used as a gate electrode material (page 385). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the gate conductor layer of WSi. One who is skilled in the art would be motivated to incorporate WSi to reduce the delays in interconnect switching.

32. Tao does not expressly disclose that the gate dielectric layer comprises SiO₂ or HfO₂. However, Tao's method is directed at patterning gate electrodes for field effect transistors (column 5, lines 56-63). Streetman teaches that in forming conventional field effect transistors, a SiO₂ gate dielectric layer is formed below the gate electrode ("G" in Figure 8-8(a), page 300). Wolf IV teaches a need for high-k dielectrics ($k > 7$) in metal-oxide-semiconductor field effect transistors, due to the increase in undesirable tunneling effects associated with thinner gate oxides, a result of device miniaturization (page 145). Wolf teaches that many important high-k materials are currently under investigation as a replacement for silicon oxide as a gate dielectric, including HfO₂ (page 145-46). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the gate dielectric layer of SiO₂ or HfO₂. One who is skilled in the art would be motivated to form a conventional structure with SiO₂, because such a structure has been successfully implemented as an operational semiconductor device. Furthermore, one who is skilled in the art would be motivated to

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find a high-k material replacement for silicon oxide, such as HfO_2 , as a gate dielectric to reduce the undesirable tunneling effects.

Claim Rejections - 35 USC § 103

33. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tao in view of Wolf I, in further view of Zhou et al. (U.S. Patent No. 5,858,847).

34. As to claim 16, Tao does not expressly disclose that the mask comprises a material selected from a group consisting of SiON , SiO_2 , Si_3N_4 , HfO_2 and α -carbon. Tao discloses that the hard masking material may be formed of those conventional in the art (column 7, lines 35-47). Zhou teaches that in forming a field effect transistor (column 1, lines 37-43), hard mask (22) is formed over the field oxide region (12) (column 3, lines 8-10). Hard mask (22) is used as both an etch barrier to etch the gate electrode (19) and as a mask to form the source and drain regions by ion implantation (column 3, lines 20-25). Moreover, Zhou teaches that hard mask (22) can be formed of silicon oxide, silicon nitride or silicon oxynitride (column 4, lines 40-45). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the mask of a material selected from a group consisting of SiON , SiO_2 , Si_3N_4 , HfO_2 and α -carbon. One who is skilled in the art would be motivated to select a conventional hard mask material that can also be used as an ion implantation mask.

Claim Rejections - 35 USC § 103

35. Claims 31 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tao, in view of Wolf I, in further view of Callister, *Materials Science and Engineering*, 4th ed., John Wiley & Sons (1997).

36. As to claims 31 and 33, Tao does not expressly disclose mathematically processing the measurements from the number of regions to create the result utilized in the adjusting step. However, Callister, as a general teaching reference, teaches that even the most precise measuring instruments produce scatter or variability in the data collected (page 135). Moreover, in order to obtain a typical value for scattered or variable data, the average value of the data (or mathematically processing the measurements) is commonly taken (page 136). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to mathematically processing the measurements from the number of regions to create the result utilized in the adjusting step. One who is skilled in the art would be motivated to use a commonly employed averaging in order to obtain a typical value for otherwise scattered or viable data. Moreover, one who is skilled in the art would be motivated to use typical data rather than scattered data in the adjusting step.

Response to Arguments

37. Applicant's arguments (Applicants' Remarks, pages 11-12), filed Sept. 6, 2005, with respect to the provisional rejection of claims 1 and 7-10 under the judicially created doctrine of double-patenting over claims 8-9, 11, and 13-14 of Mui have been fully

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considered and are persuasive. Applicants have correctly pointed out that the claim 8 of Mui does not teach or suggest adjusting a process recipe for an overetch step of an etch process that forms the structure on the substrate (page 12). The provisional rejection of claims 1 and 7-10 has been withdrawn.

38. Applicant's arguments (Applicants' Remarks, pages 12-13), filed Sept. 6, 2005, with respect to the provisional rejection of claims 12 and 19-23 under the judicially created doctrine of double-patenting over claims 16-17, 19, 21, and 23-27 of Mui have been fully considered and are persuasive, as discussed above. The provisional rejection of claims 12 and 19-23 has been withdrawn.

39. Applicant's arguments (Applicants' Remarks, pages 13-14), filed Sept. 6, 2005, with respect to the rejection of claims 1-13, 15, and 17-23 under 35 U.S.C. 102(e) as being anticipated by Tao have been fully considered and are persuasive. Applicants have correctly point out that the Tao reference does not recite using an etch process having an overetch step (page 13). Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Wolf I.

40. Applicant's arguments (Applicants' Remarks, pages 14-15), filed Sept. 6, 2005, with respect to the rejection of claim 14 under 35 U.S.C. 103(a) as being unpatentable over Tao, in view of Wolf I, in further view of Wolf IV, in further view of Streetman, have been fully considered and are persuasive, as discussed above. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Wolf I.

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41. Applicant's arguments (Applicants' Remarks, page 15), filed Sept. 6, 2005, with respect to the rejection claim 16 under 35 U.S.C. 103(a) as being unpatentable over Tao, in view of Wolf I, in further view of Streetman, in further view of Zhou, have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Wolf I.

Conclusion

42. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric B. Chen whose telephone number is (571) 272-2947. The examiner can normally be reached on Monday through Friday, 8AM to 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine G. Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EBC
Oct. 19, 2005

NADINE G. NORTON
SUPERVISORY PATENT EXAMINER
Nadine